

CLAIMS

What is claimed is:

- 1 1. A processing element comprising:
2 an instruction buffer;
3 a first most often (MO) buffer coupled to the instruction buffer; and
4 an execution unit coupled to the instruction buffer and the first MO buffer,
5 wherein the execution unit is adaptable to execute instructions stored within the first MO
6 buffer based upon a first predetermined profile.
- 1 2. The processing element of claim 1 further comprising a second MO buffer
2 coupled to the instruction buffer and the execution unit, wherein the execution unit is
3 adaptable to execute instructions stored within the second MO buffer based upon a
4 second predetermined profile.
- 1 3. The processing element of claim 2 further comprising a decode module coupled to
2 the second most often (MO) buffer coupled to the instruction buffer, the first MO buffer,
3 the second MO buffer and the execution unit.
- 1 4. The processing element of claim 3 wherein the decode module determines
2 whether an instruction is to be stored in the first MO buffer or the second MO buffer
3 upon decoding the instruction.
- 1 5. The processing element of claim 4 further comprising:
2 a first profile buffer coupled to the first MO buffer, wherein the first profile buffer
3 stores the first predetermined profile; and
4 a second profile buffer coupled to the second MO buffer, wherein the second
5 profile buffer stores the second predetermined profile.
- 1 6. The processing element of claim 5 wherein the first and second predetermined

2 profiles each include a plurality of profile bits, each profile bit indicating whether a
3 corresponding instruction is to be executed at the execution unit during a particular
4 instruction fetch cycle.

1 7. The processing element of claim 6 further comprising:
2 a first profile pointer coupled to the first profile buffer; and
3 a second profile pointer coupled to the second profile buffer.

1 8. The processing element of claim 7 wherein the first profile pointer points to a first
2 profile bit of the first predetermined profile during a first instruction fetch cycle.

1 9. The processing element of claim 8 wherein an instruction stored in the first MO
2 buffer is executed at the execution unit during the first instruction fetch cycle if the first
3 profile bit is active.

1 10. The processing element of claim 8 wherein an instruction stored in the instruction
2 buffer is executed at the execution unit during the first instruction fetch cycle if the first
3 profile bit is inactive.

1 11. A digital signal processor (DSP) comprising:
2 a plurality of processing elements, wherein each of the processing elements
3 comprises:
4 an instruction buffer;
5 a first most often (MO) buffer coupled to the instruction buffer; and
6 an execution unit coupled to the instruction buffer and the first MO buffer,
7 wherein the execution unit is adaptable to execute instructions stored within the first MO
8 buffer based upon a first predetermined profile.

1 12. The DSP of claim 11 wherein each processing element further comprises a second
2 MO buffer coupled to the instruction buffer and the execution unit, wherein the execution

3 unit is adaptable to execute instructions stored within the second MO buffer based upon a
4 second predetermined profile.

1 13. The DSP of claim 12 wherein each processing element further comprises a decode
2 module coupled to the second most often (MO) buffer coupled to the instruction buffer,
3 the first MO buffer, the second MO buffer and the execution unit.

1 14. The DSP of claim 13 wherein the decode module determines whether an
2 instruction is to be stored in the first MO buffer or the second MO buffer upon decoding
3 the instruction.

1 15. The DSP of claim 14 wherein each processing element further comprises:
2 a first profile buffer coupled to the first MO buffer, wherein the first profile buffer
3 stores the first predetermined profile; and
4 a second profile buffer coupled to the second MO buffer, wherein the second
5 profile buffer stores the second predetermined profile.

1 16. The DSP of claim 5 wherein the first and second predetermined profiles each
2 include a plurality of profile bits, each profile bit indicating whether a corresponding
3 instruction is to be executed at the execution unit during a particular instruction fetch
4 cycle.

1 17. The DSP of claim 16 wherein each processing element further comprises:
2 a first profile pointer coupled to the first profile buffer; and
3 a second profile pointer coupled to the second profile buffer.

1 18. The DSP of claim 17 wherein the first profile pointer points to a first profile bit of
2 the first predetermined profile during a first instruction fetch cycle.

1 19. A method comprising:

2 receiving a first instruction at an instruction buffer;
3 determining whether the first instruction has been designated to be retrieved from
4 a first buffer in order to be executed; and
5 if so, retrieving the first instruction from the first buffer;
6 otherwise, retrieving the buffer from a second buffer.

1 20. The method of claim 19 further comprising executing the first instruction after it
2 has been retrieved from the first buffer.

1 21. The method of claim 19 further comprising:
2 determining whether the first instruction has been designated to be stored in the
3 first buffer if the first instruction has not been designated to be retrieved from the first
4 buffer in order to be executed;
5 if so, storing the first instruction in the first buffer; and
6 executing the first instruction after it has been retrieved from the second buffer.

1 22. The method of claim 21 further comprising:
2 determining whether the first instruction includes a command to load a profile if
3 the first instruction has not been designated to be stored in the first buffer;
4 if so, loading the profile in a third buffer; and
5 executing the first instruction after it has been retrieved from the first buffer.

1 23. The method of claim 22 further comprising executing the first instruction after it
2 has been retrieved from the second buffer if it is determined that the first instruction does
3 not include a command to a load a profile if the first instruction has not been designated
4 to be stored in the first buffer.

1 24. An article of manufacture including one or more computer readable media that
2 embody a program of instructions, wherein the program of instructions, when executed

3 by a processing unit, causes the processing unit to:

4 receive a first instruction at an instruction buffer;

5 determine whether the first instruction has been designated to be retrieved from a
6 first buffer in order to be executed; and

7 if so, retrieve the first instruction from the first buffer;

8 otherwise, retrieve the first instruction from a second buffer.

1 25. The method of claim 24 wherein the program of instructions, when executed by a
2 processing unit, further causes the processing unit to execute the first instruction after it
3 has been retrieved from the first buffer.

1 26. The method of claim 24 wherein the program of instructions, when executed by a
2 processing unit, further causes the processing unit to:

3 determine whether the first instruction has been designated to be stored in the first
4 buffer if the first instruction has not been designated to be retrieved from the first buffer
5 in order to be executed;

6 if so, store the first instruction in the first buffer; and

7 execute the first instruction after it has been retrieved from the second buffer.

1 27. The method of claim 26 wherein the program of instructions, when executed by a
2 processing unit, further causes the processing unit to:

3 determine whether the first instruction includes a command to load a profile if
4 the first instruction has not been designated to be stored in the first buffer;

5 if so, load the profile in a third buffer; and

6 execute the first instruction after it has been retrieved from the first buffer.

1 28. The method of claim 27 wherein the program of instructions, when executed by a
2 processing unit, further causes the processing unit to execute the first instruction after it
3 has been retrieved from the second buffer if it is determined that the first instruction does

- 4 not include a command to a load a profile if the first instruction has not been designated
- 5 to be stored in the first buffer.

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